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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/933,468	08/20/2001	Christopher S. MacLellan	EMC-01-018	5620

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EXAMINER	
TABONE JR, JOHN J	
ART UNIT	**PAPER NUMBER**
2138	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/01/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/933,468	MACLELLAN, CHRISTOPHER S.	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claim 1-24 remain pending in the current application and have been examined.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/04/2006 has been entered.

Response to Arguments

3. Applicant's arguments and Affidavit under 37 C.F.R. 1.131, filed 11/06/2006 and 12/04/2006, with respect to the rejected claims 1-24 have been fully considered and are persuasive. Therefore, the Final Rejection of 09/06/2006 has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Jamal (US-5572712).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 2, 6-8, 13, 14, and 18-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Jamal (US-5572712), hereinafter Jamal.

Claims 1, 2, 13 and 14:

Jamal teaches a first logic section (**BIST circuit 40 - Address Generator 48 and clock and control signal generator 52, BIST logic** as per claims 2 and 14) that may transmit one or more test-related signals (**The clock and control signal generator 52 is the heart of the BIST circuit 40. It generates internal clock signals, address direction signals, read/write enable signals, MISR clock signals, test patterns, and an end-of-test signal for the RAM 42**) for use during a test mode of the SUT (**RAM 42**). Jamal also teaches **a second logic section** (**other components of the IC die 32**) that may transmit one or more other signals (**system signals**) during a normal operating mode of the SUT (**RAM 42**). Jamal further teaches a third logic section that selectively couples the first logic section or the second logic section to the SUT (**[t]he initialization logic 46 commands the multiplexer 44 to decouple the RAM 42 from the other components of the integrated circuit die 32** (the second logic section) **and couples the BIST 40** (the first logic section) **to the RAM**) based upon respective states of two control signals, one of the two control signals being transmitted to the third logic

section from a source that is external to the SUT (**test mode enable signal**), the first logic section, the second logic section, and the third logic section, the other of the two control signals being transmitted to the third logic section from the first logic section (**control signal from clock and control signal generator 52 to the multiplexer 44**). Jamal discloses when the third logic section couples the first logic section to the SUT, the first logic section transmits the one or more test-related signals to the SUT, and when the third logic section couples the second logic section to the SUT, the second logic section may transmit the one or more other signals to the SUT. (Col. 5, ll. 6-45, Fig. 3).

Claims 6 and 18:

Jamal teaches the respective assertion state of the one of the two control signals (**test mode enable signal**). (Col. 5, ll. 6-45, Fig. 3).

Claims 7 and 19:

Jamal teaches when the third logic section (**initialization logic 46 and the multiplexer 44**) couples the first logic section (**BIST 40**) to the SUT (**RAM 42**), the first logic section (**BIST 40, in particular MISR 50**) may receive one or more test outputs from the SUT (**DO from RAM 42**), the one or more test output signals being generated by the SUT in response to the one or more test-related signals, and the first logic section may compare the one or more test outputs (**signature comparator 54**) to one or more expected test outputs whereby to determine results of the testing. (Col. 4, l. 64 to col. 5, l. 5, col. 5 l. 46 to col. 6, l. 11, Fig. 3).

Claims 8 and 20:

Jamal further teaches a third logic section that selectively couples the first logic section or the second logic section to the SUT (**[t]he initialization logic 46 commands the multiplexer 44 to decouple the RAM 42 from the other components of the integrated circuit die 32** (the second logic section) **and couples the BIST 40** (the first logic section) **to the RAM**) based upon respective states of two control signals as per the rejection of claims 1 and 13 above. Jamal also teaches in "normal" or "functional mode" (**i.e. test mode enable unasserted**), the BIST circuit 40 permits a transparent interaction between other components of the integrated circuit die 32 and the RAM 42 through the multiplexer logic 44 (**If at least one of the control signals is unasserted...**). Jamal further teaches the BIST circuitry 40 switches to test mode upon receipt of a "test mode" or "test enable" signal along with a test clock signal. (**if both control signals are asserted...**). (Col. 4, l. 64 to col. 5, l. 46).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 10, 11, 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jamal (US-5572712), hereinafter Jamal.

Claims 10 and 22:

Jamal teaches all the claimed limitations of claims 10 and 22 as per the rejection of claims 1 and 13 above. As such, in the language of claims 10 and 22, Jamal teaches a first logic section (**BIST circuit 40 - Address Generator 48 and clock and control signal generator 52, BIST logic** as per claims 2 and 14) that may transmit one or more test-related signals (**The clock and control signal generator 52 is the heart of the BIST circuit 40. It generates internal clock signals, address direction signals, read/write enable signals, MISR clock signals, test patterns, and an end-of-test signal for the RAM 42**) for use during a test mode of the SUT (**RAM 42**). Jamal also teaches a second logic section (**other components of the IC die 32**) that may transmit one or more other signals (**system signals**) during a normal operating mode of the SUT (**RAM 42**). Jamal further teaches a third logic section that selectively couples the first logic section or the second logic section to the SUT (**[t]he initialization logic 46 commands the multiplexer 44 to decouple the RAM 42 from the other components of the integrated circuit die 32** (the second logic section) **and couples the BIST 40** (the first logic section) **to the RAM**) based upon respective states of two control signals, one of the two control signals being transmitted to the third logic section from a source that is external to the SUT (**test mode enable signal**), the first logic section, the second logic section, and the third logic section, the other of the two control signals being transmitted to the third logic section from the first logic section (**control signal from clock and control signal generator 52 to the multiplexer 44**). Jamal discloses when the third logic section couples the first logic section to the SUT, the first logic

section transmits the one or more test-related signals to the SUT, and when the third logic section couples the second logic section to the SUT, the second logic section may transmit the one or more other signals to the SUT. (Col. 5, ll. 6-45, Fig. 3).

Jamal does not explicitly teach "**a plurality of second logic sections**" and "**a plurality of third logic sections**". However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to duplicate Jamal's second logic section (**other components of the IC die 32**) and third logic section (**initialization logic 46 and the multiplexer 44**). Also, it would have been obvious to one of ordinary skill in the art at the time the invention was made because it is well known the art that a system such as Jamal's has multiple memories (**ROM 20 and RAM 22 of Fig. 1**) which all have to be tested. The artisan would be motivated to do so since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8 (7th Cir. 1977).

Claims 11 and 23:

Jamal teaches the testing system is comprised in an application specific integrated circuit (ASIC) (**integrated circuit die 32**), and the source is external to the ASIC (**test mode enable signal from TAP controller**). (Fig. 3, Col. 5, ll. 6-45).

6. Claims 3-5, 12, 15-17 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jamal (US-5572712), hereinafter Jamal, in view of Miner (US-6370661), hereinafter Miner.

Claims 3 and 15:

Jamal does not explicitly teach that "the first logic section (**BIST circuit 40 - Address Generator 48 and clock and control signal generator 52**) provides an indication signal to the second logic section (**other components of the IC die 32**) for indicating when the first logic section (**BIST circuit 40**) is attempting to test the SUT (**RAM 42**)". Miner teaches in an analogous art a configurable (programmable) BIST architecture that dynamically interacts with a test controller (I/O controller). Miner also teaches the test sequences within the test management logic 570 (BIST) are configurable. More specifically, the test sequences that are designed into the test management logic 570 (BIST) are non-specific, that is, they can be configured with test parameters, provided by the test controller 580, to execute accesses to any memory 510, within any address range, to read or write any data pattern. The test management logic 570 accepts test parameters in a configuration register 572 that are transferred from the test controller 580 (I/O controller) over the test control bus 575 and the results of a test sequence can be accessed by the test controller 580 (I/O controller) in result register 573. In one embodiment, the configuration register 572 and the result register 573 are JTAG registers. Miner further teaches test execution logic 560 (also part of BIST) directly drives address, data, and control signals on the local bus 532 to directly access each of the memories 510. Miner also discloses prior to executing a test sequence, the test execution logic 560 sends a test signal 565 to the bus unit 530 (**an indication signal to the second logic section**) to preclude contention on the local bus

532, thus effectively disabling the bus unit 530 during testing. (Col. 9, l. 51 to col. 11, l. 55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Jamal's BIST circuit 40 (**Address Generator 48 and clock and control signal generator 52**) with Miner's configurable (programmable) BIST architecture. The artisan would be motivated to do so because it would enable Jamal's BIST circuit 40 to send a test signal 565 (**an indication signal**) to the bus unit 530 (**the second logic section**, i.e. Jamal's other components of the IC die 32) to preclude contention on the local bus 532, thus effectively disabling the bus unit 530 during testing (**for indicating when the first logic section (BIST circuit 40) is attempting to test the SUT (RAM 42)**). (see Miner, col. 11, ll. 47-55).

Claims 4 and 16:

Jamal in view of Miner discloses the second logic provides to the I/O controller (**test controller 580**) an indication that the testing of the SUT (**RAM 42**) is occurring (**a test signal 565**). Jamal in view of Miner also discloses the I/O controller (**test controller 580**) is external to the first logic section (**BIST circuit 40**), the second logic section (**other components of the IC die 32, bus unit 530**), the third logic section (**initialization logic 46 and the multiplexer 44**), and the SUT (**RAM 42**). (see Miner, Col. 9, l. 51 to col. 11, l. 55).

Claims 5 and 17:

Jamal in view of Miner discloses prior to executing a test sequence, the test execution logic 560 sends a test signal 565 (**an indication signal**) to the bus unit 530

(**the second logic section**) to preclude contention on the local bus 532, thus effectively disabling the bus unit during testing 530 (**data transfer to be invalidated**). (see Miner, Col. 11, ll. 21-24).

Claims 12 and 24:

The coupling of the first logic section to each of the third and second logic sections is rejected as per claims 10 and 22 above. Jamal does not explicitly teach that the BIST circuit 40 is "programmable". However, Jamal does teach that BIST 40 requires an initialization. (Col. 5, ll. 21-34). Miner teaches in an analogous art a configurable (programmable) BIST architecture that dynamically interacts with a test controller. Miner also teaches the test sequences within the test management logic 570 (BIST) are configurable. More specifically, the test sequences that are designed into the test management logic 570 (BIST) are non-specific, that is, they can be configured with test parameters, provided by the test controller 580, to execute accesses to any memory 510, within any address range, to read or write any data pattern. The test management logic 570 accepts test parameters in a configuration register 572 that are transferred from the test controller 580 over the test control bus 575 and results of a test sequence can be accessed by the test controller 580 in a result register 573. In one embodiment, the configuration register 572 and the result register 573 are JTAG registers. Miner further teaches test execution logic 560 (also part of BIST) directly drives address, data, and control signals on the local bus 532 to directly access each of the memories 510. (Col. 9, l. 51 to col. 11, l. 55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Jamal's BIST circuit 40 with Miner's configurable (programmable) BIST architecture. The artisan would be motivated to do so because it would enable Jamal to allow an operator full flexibility through the test controller 580 to configure any specific sequence of memory accesses to a memory 510. (see Miner, col. 11, ll. 47-55).

7. Claims 9 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jamal (US-5572712), hereinafter Jamal, in view of Walker (US-6539503), hereinafter Walker.

Claims 9 and 21:

Jamal teaches the SUT is a memory (**RAM 42**). (Col. 5, ll. 6-45, Fig. 3). Jamal does not explicitly teach "the second section transmits an erroneous value to be stored in the memory that is detected during a second test mode of the system". Walker teaches in an analogous art error injector 630 injects an error into a codeword variable (**an erroneous value to be stored in the memory**) that is prompted by a triggering condition or event. (Col. 6, ll. 24-42). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Jamal' second logic section (**other components of the integrated circuit die 32**) to include Walker's error injector 630. The artisan would be motivated to do so because it would enable Jamal the flexibility to inject errors, i.e. erroneous values, into a memory location in the cache memory for later detection by the Jamal's BIST circuit 40.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Kim et al. (US-6457141) substantially teaches the first, second and third logic sections as claimed.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

John J. Tabone, Jr.
Examiner
Art Unit 2138

1/24/07

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